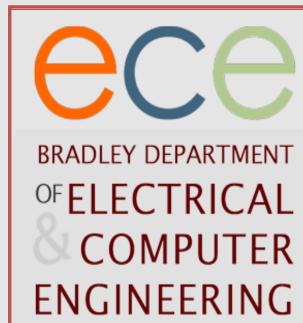
## A PREVIEW OF THE OPENPR OPEN-SOURCE PARTIAL RECONFIGURATION TOOLKIT FOR XILINX FPGAS



Virginia Tech Configurable Computing Lab www.ccm.ece.vt.edu

Passthroughs

routeBlocker

Route Static

Design

Remove

Passthroughs

and blocking

routes

bitgen

Static Bitstream

Blocking Routes

Static Routes

Static Region

**USC Information Sciences Institute** www.east.isi.edu Aaron Wood

bitgen

Full Bitstreams

for Partial

Designs

partialGenerator

Partial

Bitstreams



PR Module

Bus Macros

## Ali Sohanghpurwala and Peter Athanas COMPUTER {asohangh,athanas}@vt.edu awood@east.isi.edu Information Sciences Institute Objectives Overview **Necessary PR Components** Partial Board Module based Partial Reconfiguration Toolkit Exclusion: Interface: Static HDL Modules HDL Constraints Define spatially Keep static Slot-based flow similar to 9.2PR routing/logic out of consistent routing Works on top of any version of Xilinx Tools PR Region terminals Release source code so that researchers can OpenPR Confinement: extend functionality Partial Bitstream Constraint all dynamic Xilinx ISE Tools Support V4/V5 initially but easily expandable Generation (Any Version) routing/logic to PR to other architectures Region STATIC DESIGN FLOW PARTIAL MODULE FLOW Partial Static Bitstream Bitstreams Partial Modules PR Region Static HDL HDL Physical Resource Estimates xst xst Partial Design Floorplanning Confinement Route Build Define Dynamic Place with ISE Region tools Placed Logic Empty Fabric BusMacro routeBlocker ukegnon Locations Static Design Build **Route Partial** siteBlocker Design Region Place with ISE Remove tools Static Region Confinement Routes Route Bus Macro

Static Clocktree